A DC-to-40 GHz Four-Bit RF MEMS True-Time Delay Network

M. Kim, *Member, IEEE*, J. B. Hacker, *Member, IEEE*, R. E. Mihailovich, *Member, IEEE*, and J. F. DeNatale

***Abstract*—A monolithic true-time delay (TTD) network containing sixteen metal-to-metal contact RF microelectromechanical systems (MEMS) switches has been successfully fabricated and characterized. The TTD network was designed to produce flat delay time over a dc-to-40 GHz bandwidth with full 360-degree phase control at 22.5-degree intervals at 10.8 GHz. Measurements show a close match to the designed delay times for all sixteen switch states with 2.2 to 2.6 dB of insertion loss at 10 GHz. The worst group delay ripple in the dc-to-30 GHz range was 3 ps, well within the single bit delay time of 5.8 ps.**

***Index Terms*—MEM relay, phase shifter, RF MEMS switch, true-time delay.**

I. INTRODUCTION

WIDE-BANDWIDTH radar systems acquiring frequency-dependent target response and multi-path characteristics demand phase shifters with minimum frequency dispersion. Switched-line true-time delay networks utilizing RF microelectromechanical systems (MEMS) switches can meet these needs. Such networks can provide accurate phase control over a broad frequency range of several octaves with minimum RF power loss and at greatly reduced weight and cost. Difficulties in fabrication of direct metal-to-metal contact MEMS switches, however, have made fabricating such a TTD network impractical until now. Consequently, most published MEMS phase shifters have adopted a different approach based on capacitive switches [1]. A capacitive switch, normally suspended over a RF through-line forming a bridge between two ground planes, presents a shunt reactance to the RF signal line. Using such switches, Raytheon demonstrated X-band four-bit reflection phase shifters with two Lange couplers [2] and resonant delay-line phase shifters at Ka-band [3]. These phase shifters showed good insertion loss, but suffered from narrow bandwidth and sizable phase offset errors. Another highly publicized MEMS phase shifter [4] uses a CPW line with distributed MEMS bridges in order to vary the phase velocity of the line. In this case, the pull-down voltage restriction permits only small variations of the bridge capacitance such that the maximum delay-change is only 4 ps for an 87-ps line. The TTD network presented here overcomes these limitations to achieve performance and bandwidth that exceed those based on capacitive switches.

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M. Kim was with Rockwell Science Center, Thousand Oaks, CA 91358. He is now with Electrical Engineering Department, Korea University, Seoul 136-701, Korea (mkim@rsc.rockwell.com).

J. B. Hacker, R. E. Mihailovich, and J. F. DeNatale are with Rockwell Science Center, Thousand Oaks, CA 91358 (e-mail: remihailovich@rsc.rockwell.com).

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Recent progress on metal-to-metal contact MEMS switches developed at Rockwell Science Center [5] has enabled fabrication of high-quality switched-line true-time delay networks for the first time. These switches use a movable metal shunting bar to connect two RF signal lines when the dc activation voltage of 70 V is applied. Measurements on discrete Rockwell switches show typical dc/RF contact-resistances of $2 \times 0.5\ \Omega$ while the off-switch coupling capacitance is only 1.75 fF. Switch fabrication has reached a level of maturity that switch yield and uniformity are now sufficient to construct a four-bit TTD network.

II. TTD IMPEDANCE MATCHING

In order to characterize the four-bit TTD network without the complexity of the entire circuit, the second longest bit (bit #3) was fabricated separately as a single-bit TTD circuit. Microstrip lines, 55-μm wide on a 75-μm thick GaAs substrate, were designed to provide the required time delay. Chamfered 90-degree bends were used for all corners in the delay line to minimize reflections. Two tee-junctions, each containing two MEMS switches, were used to route the signal through the desired delay path. Rockwell MEMS switches have the RF signal-line sandwiched by two $100 \times 100\ \mu\text{m}^2$ drive capacitors that form the electrostatic actuators. Because the gap between the two drive capacitors is only 80 μm, the width of the signal line was narrowed to 40 μm in a 330-μm section surrounding the switch. Simulations indicate this high-impedance transmission-line section for the closed switch has almost no impact on circuit performance up to 40 GHz. A more serious mismatch, that prevents the TTD circuit from working at higher frequencies, comes from the open-stub transmission-lines connected to the open switches at the tee-junctions. An effort was made to shrink the size of the switch to reduce the open-stub length down to 176 μm. This length corresponds to a quarter-wavelength at approximately 145 GHz, so that the RF signal will be completely reflected at the tee-junction at this frequency. However, even at lower frequencies, the mismatch introduced by the open-stub transmission-line capacitance creates a resonance resulting in increased dispersion in the group-velocity. Adding an inductive microstrip matching section, 16-μm wide and 160-μm long, in series with the tee-junction reduces circuit mismatch and phase dispersion in the frequency band of interest. The matched tee-junction can be modeled by using a simple series inductor and parallel capacitor. The group delay from this circuit can be written as,

$$\tau = -\frac{d\theta}{d\omega} = \frac{d}{d\omega}\tan^{-1}\left(\frac{\omega C Z_0 + \omega L/Z_0}{2 - \omega^2 LC}\right) \tag{1}$$

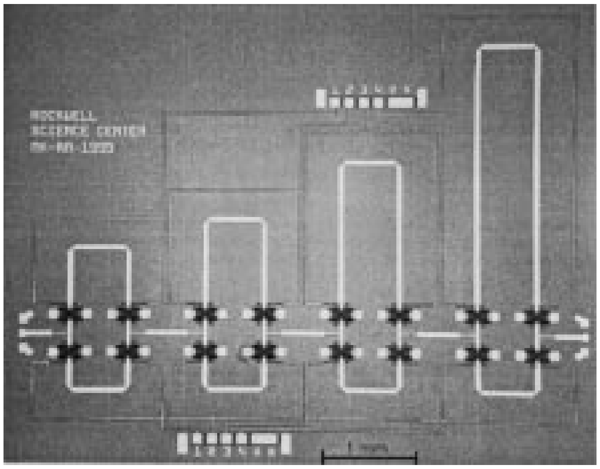

Fig. 1. Photograph of the four-bit RF MEMS TTD network. The second longest bit (bit #3) was fabricated separately to analyze both the insertion loss and the impact of the matching section on TTD performance.

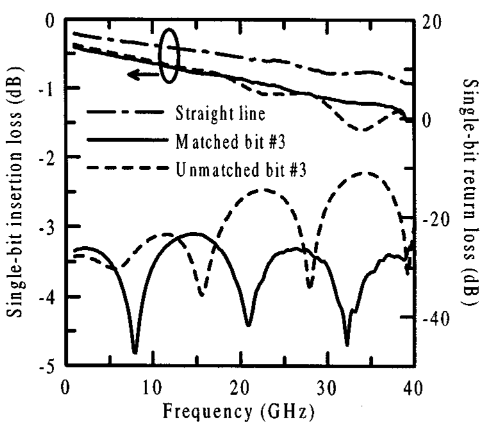

Fig. 2. Single-bit TTD test results. Insertion loss form both the matched and unmatched delay circuits are compared with the loss from a straight 40-Ω microstrip line.

where θ is the phase delay for a two-port network consisting of series inductor L and parallel capacitor C with a normalization impedance of Z_0. Generally, a reactive element degrades the delay flatness when used alone. It can be readily shown, however, that a proper choice of L can reduce the delay ripple caused by C due to the second order term in the denominator. Fig. 2 compares the performance of single-bit TTD circuits with and without the inductive matching sections. During fabrication, the wafer was accidentally thinned down to 50 μm, much less than the 75-μm substrate thickness assumed during the design. To compensate, the measured data was plotted with the input and output impedance changed to 40 Ω. Both matched and unmatched circuits show good return loss at frequencies below 15 GHz. However, above 15 GHz, the return loss for the unmatched TTD network degrades to 10 dB and ripples in the insertion loss are introduced. The measured group delay for the matched TTD network maintains a constant value with less than 1 ps ripple up to 30 GHz, whereas the delay for the unmatched TTD network oscillates with the ripple size close to 5 ps above 15 GHz.

Several passive structures were also tested at 10 GHz to isolate the switch loss from delay line loss. A straight line that produces the same delay time as the switched single-bit circuit showed 0.37 dB of conductor loss. This number matches well with the loss predicted by an Agilent Momentum simulation with a metal thickness of 2.1-μm and a conductivity of 4×10^7 S/m. A single-bit structure with fixed metal shorts in place of the MEMS switches showed 0.47 dB of loss. The extra 0.1 dB of loss was due to line bends and tee-junctions. The insertion loss of the single-bit circuit with MEMS switches was 0.63 dB at 10 GHz indicating roughly 0.08 dB of loss and a 2×0.4 Ω contact resistance per switch.

III. Four-Bit TTD Performance

Sixteen different sets of switch positions for the matched and unmatched four-bit TTD networks were tested using an on-wafer RF probe station. The monolithic TTD network employing sixteen MEMS switches (Fig. 1), 6×5 mm^2 in size, was designed to produce delay times from 106.9 to 193.9 ps at 5.8 ps intervals over a dc-to-40 GHz frequency range. The delay time step corresponds to 22.5 degrees of phase shift at 10.8 GHz and is realized with 600 μm-long delay lines. As in the single-bit case, the system impedance was renormalized to 40 Ω because of the reduced substrate thickness. Eight separate dc bias lines, carrying either 0 V or 98 V, were used to control the switch positions. To ensure good metal-to-metal contact for all eight switches for a chosen delay path, a higher than normal dc voltage was applied. Fig. 3 shows the performance of both matched and unmatched four-bit TTD networks. For the matched TTD network, the variation in insertion loss for all sixteen states was only 0.4 dB (from 2.2 to 2.6 dB) at 10 GHz and 0.7 dB (from 3.6 to 4.3 dB) at 30 GHz. The return loss was better than 20 dB for all delay states over most of the frequency band [Fig. 3(a)]. The plot shown in Fig. 3(b) shows both linearity and the amount of phase shift achieved from the matched TTD network. The phase difference between the shortest and the longest paths was 343 degrees at 10.8 GHz. The unmatched TTD network displayed an almost identical amount of phase shift. The linearity of the phase shift can be more accurately described by the group delay time plotted in Fig. 3(c). Group delay times produced by the unmatched TTD network stay flat up to 15 GHz, but start overlapping with delay times from other states at higher frequencies. On the other hand, the matched TTD network maintains clearly distinguishable flat delay times up to 40 GHz. The ripple in the delay time for the matched TTD network over the dc-to-30 GHz frequency bandwidth is approximately 2 ps for the shortest delay path and 3 ps for the longest delay path. The delay time ripple increases rapidly by up to 7 ps in the 30-to-40 GHz range.

The performance of the four-bit TTD is summarized in Fig. 3(d). The difference in group delay times for each state match closely with the designed delay times. At 10 GHz, the largest deviation from the designed delay times was about 0.8 ps. The measured insertion loss at 10 GHz for all sixteen states also matches well with the predicted loss numbers when 0.1 dB-per-switch loss was added to the estimated conductor losses from the delay lines.

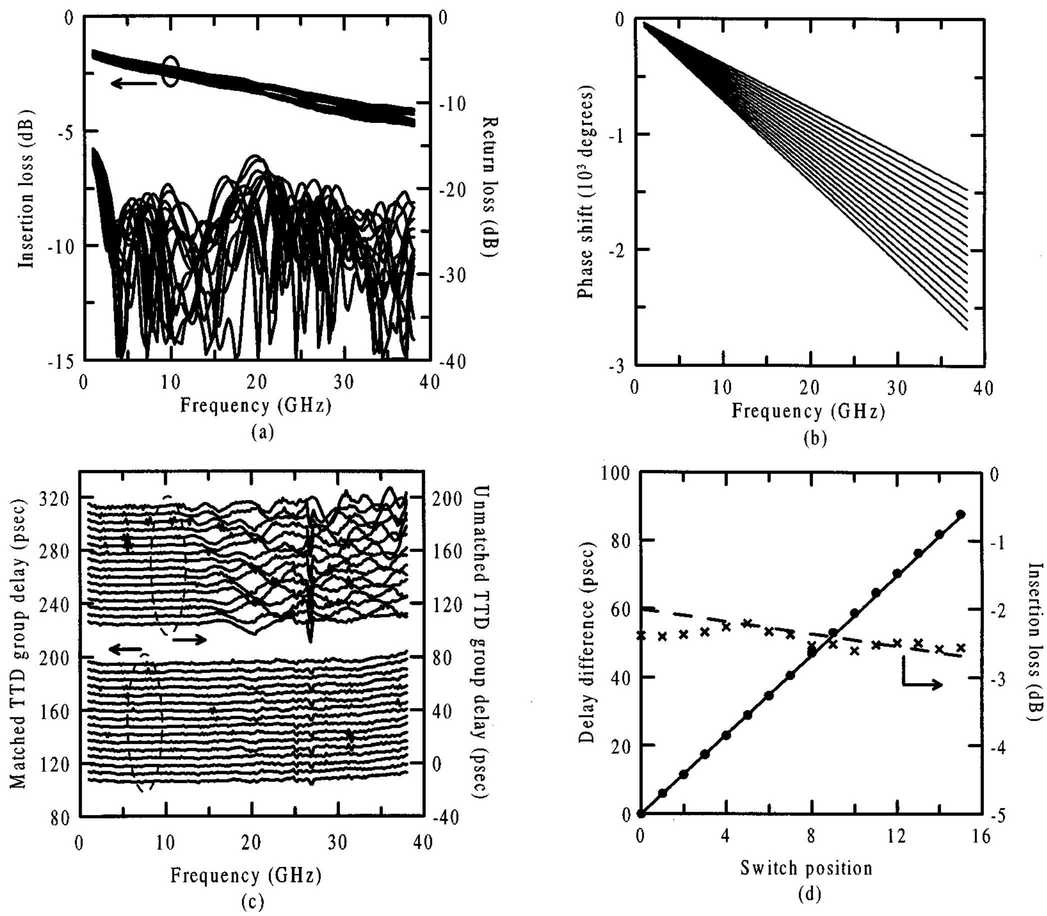

Fig. 3. Performance of the four-bit TTD network. (a) The insertion loss and return loss and (b) phase shift from a matched TTD network are shown. (c) Group delay times for the matched and unmatched TTD network. (d) Comparison of the matched TTD network performance at 10 GHz with theory (shown as lines).

IV. Conclusions

Two types of four-bit TTD networks with direct metal-to-metal contact MEMS switches have been successfully fabricated for the first time. Switch yield was excellent as was switch contact uniformity at $2 \times 0.5\ \Omega$ per switch. TTD performance was greatly enhanced by inserting a simple high-impedance matching section. Nearly flat delays up to 40 GHz for all sixteen switch states were achieved.

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